

Fast CMOS 3.3V 16-Bit Registered Transceivers

Product Features

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability: Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

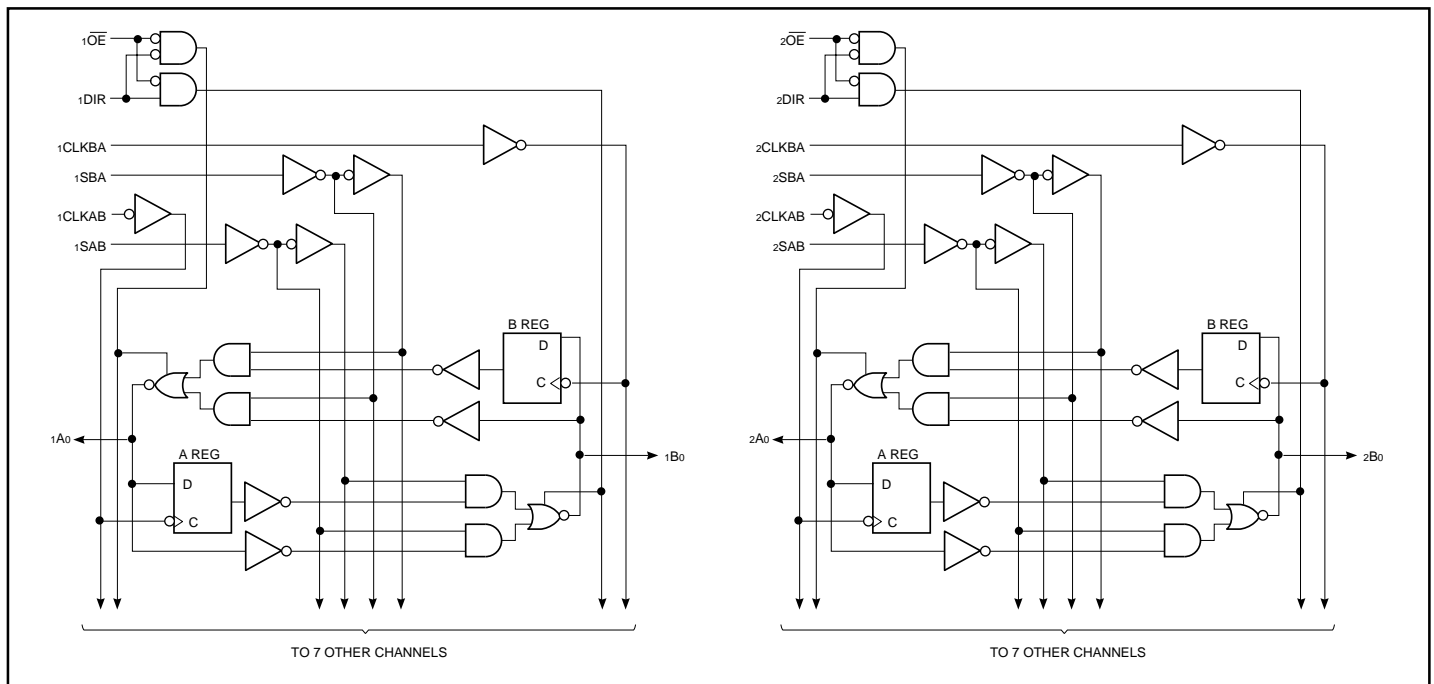
Product Description

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16646 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers designed with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control (\overline{xOE}) and direction pins (\overline{xDIR}) to control the transceiver functions. The Select (\overline{xSAB} and \overline{xSBA}) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74LPT16646 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

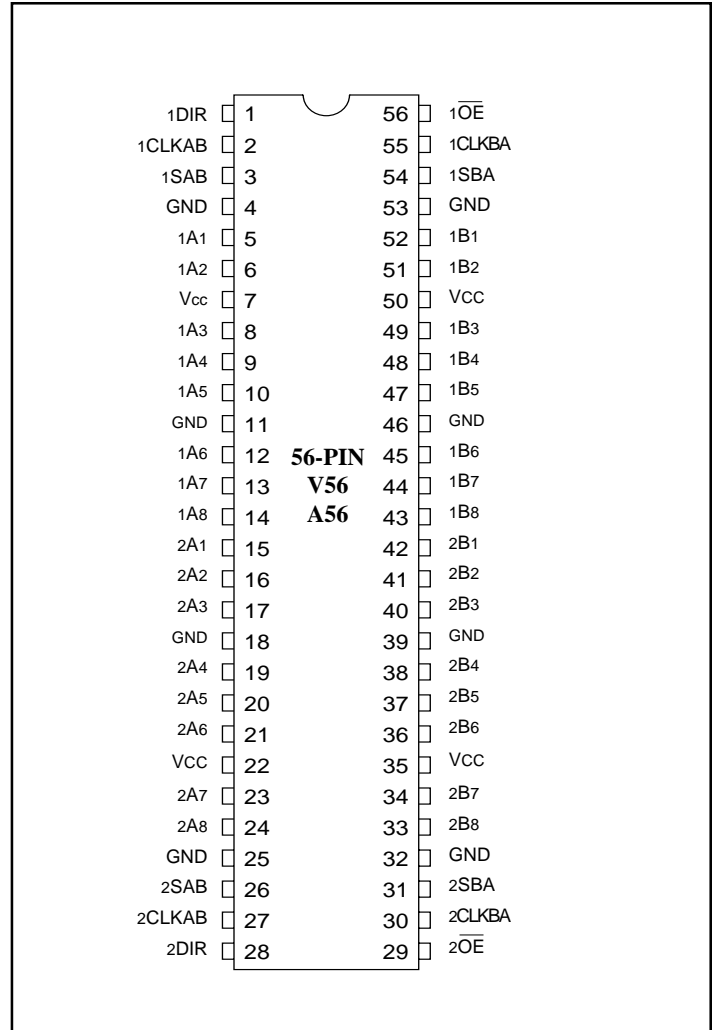
Logic Block Diagram



Product Pin Description

Pin Name	Description
x \overline{OE} , xDIR	Output Enable Inputs (Active LOW)
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
GND	Ground
Vcc	Power

Product Pin Configuration

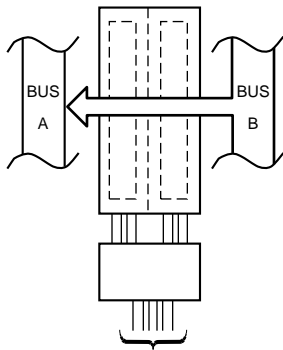


Truth Table⁽²⁾

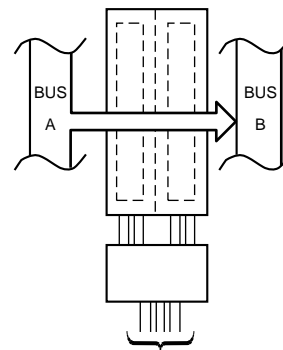
Function	Inputs						Data I/O ⁽¹⁾	
	x \overline{OE}	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

Note:

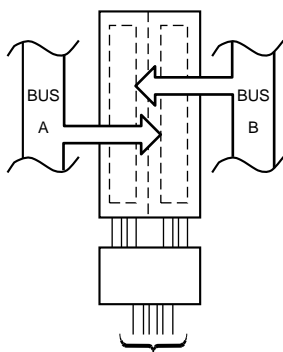
- The data output functions may be enabled or disabled by various signals at the x \overline{OE} or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, ↑ = LOW-to-HIGH Transition

**REAL-TIME TRANSFER
BUS B TO A**


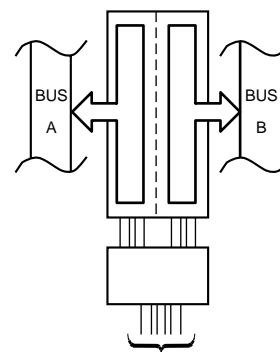
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

**REAL-TIME TRANSFER
BUS A TO B**


xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

**STORAGE FROM
A AND/OR B**


xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

**TRANSFER STORES
DATA TO A AND/OR B**


xDIR ⁽¹⁾	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Note:

1. Cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ...	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max.	VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	VCC = Max.	VIN = VCC	—	—	±1	µA
IIL	Input LOW Current (Input pins)	VCC = Max.	VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	VCC = Max.	VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current (3-State Output pins)	VCC = Max.	VOUT = 5.5V	—	—	±1	µA
IOZL		VCC = Max.	VOUT = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min.	IOH = -0.1 mA	VCC-0.2	—	—	V
		VIN = VIH or VIL	IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL	IOH = -8 mA IOH = -24 mA	2.4 ⁽⁵⁾ 2.0	3.0 —	— —	V
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 0.1 mA	—	—	0.2	V
			IOL = 16 mA	—	0.2	0.4	V
			IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V		—	—	±100	µA
VH	Input Hysteresis			—	150	—	mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} – 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{CC} – 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{CC} – 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})

ΔI_{CC} = Power Supply Current for a TTL High Input

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

N_{CP} = Number of Clock Inputs at f_{CP}

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16646		LPT16646A		LPT16646C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width ⁽⁴⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁽⁵⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance ($T_A = 25^\circ C$, $f = 1$ MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
COU	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.